**Test Log**

HW part number: HW001

HW revision: R002

Firmware version: initial, unreleased test firmware

Software version: N/A

Test case: board bringup

Test date: 2018-05-11

|  |  |
| --- | --- |
| **Test power supplies**  Apply +5V to 5V power rail.  Verify 1.2V appears at 1.2V power rail.  Verify 3.3V appears at 3.3V power rail. | Pass  Pass |
| **Verify ICSP communications**  Apply +5V to 5V power rail.  Verify 1.2V appears at 1.2V power rail.  Verify 3.3V appears at 3.3V power rail.  Verify ICSP connection succeeds. | Pass  Pass  Pass |
| **Verify FPGA configuration**  Apply +5V to 5V power rail.  Verify 1.2V appears at 1.2V power rail.  Verify 3.3V appears at 3.3V power rail.  Initiate debug session.  Verify ICSP connection succeeds.  Verify state of uFpgaResult is in main scope has a value of 1 after FPGA configuration. | Pass  Pass  Pass  Pass |
| **Test power LED**  Apply +5V to 5V power rail.  Verify 1.2V appears at 1.2V power rail.  Verify 3.3V appears at 3.3V power rail.  Verify power LED illuminates. | Pass  Pass  Pass­ |
| **Test mode LED**  Apply +5V to 5V power rail.  Verify 1.2V appears at 1.2V power rail.  Verify 3.3V appears at 3.3V power rail.  Initiate debug session  Verify ICSP connection succeeds  Verify TRIS direction register sets RB4 (mode LED, pin33) to output  Verify LATB register sets RB4 output (mode LED, pin33) to low level (0.0 - 0.7 V) | Pass  Pass  Pass  Fail  Fail |
| **Investigative notes (mode LED still not working)**  Attempt to re-write HAL GPIO subsystem to use LATXbits.LATX format.   * Observe variable view in MPLAB-X   Attempt to re-write HAL GPIO subsystem to use TRISXbits.TRISX format.   * Observe variable view in MPLAB-X   Attempt to bypass FPGA configuration and corresponding PPS configuration.  Attempt to apply 0V to LED cathode (modify fw to set pin to hi-Z).  Attempt to measure resistance between µC pin 33 and LED cathode.  Measure voltage applied by µC to turn LED on (shoud be approximately 0)  Investigation of the part (PIC24FJ128GB204) showed pin 33 is input only. | No effect  LATB4 0  No effect  TRISB4 0  No effect  No effect  680 Ω  2.2V  **Design** |

Summary

Design flaw in MODE connection shows that the port used for the LED cannot assert an output.

The CRESET connection also is input only. It is suspected that the FPGA configure test passed because the FPGA waits for configuration.

Proposed prototype fix: bridge pins 32 and 33 for MODE LED.

CRESET design defect cannot be easily resolved, so a new PCB will be needed.

HW part number: HW002

HW revision: R002

Firmware version: initial, unreleased test firmware

Software version: N/A

Test case: board bringup

Test date: 2018-05-13

|  |  |
| --- | --- |
| **Test mode LED**  Apply +5V to 5V power rail.  Verify 1.2V appears at 1.2V power rail.  Verify 3.3V appears at 3.3V power rail.  Initiate debug session  Verify ICSP connection succeeds  Verify TRIS direction register sets RB4 (mode LED, pin33) to output  Verify LATB register sets RB4 output (mode LED, pin33) to low level (0.0 - 0.7 V)  Verify Mode LED illuminates | Pass  Pass  Pass  Pass  Pass  Pass |

Summary

RB4 (MODE, pin 33) and RA4 (CRESET, pin 34) are listed as input only in the device datasheet.

Bridging pins 32 and 33, and changing MODE logic (software) from RB4 (pin 33) to RA8 (pin 32) corrects the problem.

The FPGA reports as being configured correctly. Since the device presumably cannot assert CRESET, I assume this is because the FPGA simply waits for its configuration image until the MCU provides it.